Amendments to the Claims

1. (Withdrawn)

2. (Withdrawn)

3. (Withdrawn)

4. (Withdrawn)

5. (Withdrawn)

6. (Withdrawn)

7. (Withdrawn)

8. Withdrawn)

9. (Withdrawn)

10. (Withdrawn)

11. (Withdrawn)

12. (Currently Amended) An arbitration circuit for an output port, comprising:

a FIFO queue containing a head pointer and a plurality of characterizing data for each packet received at an input port, the queue forming a look-up table to determine which data will be sent out from the output port; and

a plurality of arbitration circuits coupled to the look-up table for selecting the next packet to be sent out corresponding to a preselected characterizing datum wherein the head pointer of the selected packet is utilized to select the packet from a common memory for the plurality of arbitration circuits.

13. (Cancelled)

14. (Cancelled)

15. (Currently Amended) The arbitration circuit of Claim [[13]] 12 wherein the arbitration circuit is the arbitration circuit for one port of a PCI Express switch.

16. (Currently Amended) The arbitration circuit of Claim [[14]] 12 wherein the common memory is shared by all ports in the PCI Express switch.

17. (Original) The arbitration circuit of Claim 15 wherein the common memory is a crossbar memory.

18. (Original) The switch of Claim 16 wherein the crossbar memory is a common port, virtual channel or type memory.

19. (Currently Amended) The arbitration circuit of Claim [[14]] 12 wherein the PCI Express switch comprises:

a plurality of ports;

a plurality of port controllers, each controller being coupled to one of the ports;

a local bus coupling the port controllers to a controller subsystem; and

a single crossbar memory coupled to each of the port controllers and the controller subsystem, the crossbar memory serving as a common port or virtual channel memory for each of the port controllers.

20. (Original) The switch of Claim 18 wherein the crossbar memory is a common port, virtual channel or type memory.

21. (Original) The switch of Claim 18 wherein the crossbar memory is used as the replay memory by storing the head pointer in the port controller.